MAX14570

High-Efficiency Voice Coil Motor Driver

General Description

The MAX14570 is a high-efficiency voice coil motor (VCM) driver ideal for use in power-sensitive autofocus camera applications.

The MAX14570 utilizes a switching output topology to provide high efficiency over the entire input supply voltage range. Optional output slew-rate control and spread-spectrum oscillator reduce conducted noise and radiated emissions.

The device features a 0 to 100mA output-current range programmable with 10-bit resolution. A tunable ringing compensation filter significantly improves VCM actuator setting time, speeding up autofocus convergence time and reducing shutter lag.

Additional features include on-board diagnostics to detect/prevent open-/short-circuit conditions and a low-power shutdown mode.

The MAX14570 is available in a 0.78mm x 1.35mm x 0.35mm, 6-bump WLP package with 0.4mm pitch.

Applications

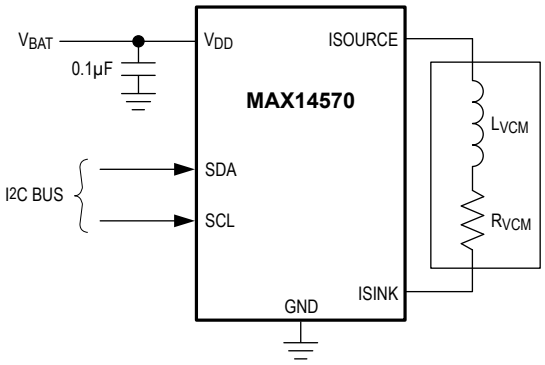
- VCM-Based Autofocus Actuator Drives
- Autofocus Cellular Phone Camera Modules

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Flexible VCM Driver Design
  - Selectable PWM or Linear Mode Output
  - High-Efficiency Class-D Output Stage ~80% Efficiency at 60mA Output Current (V_{DD} = 2.8V)
- I²C-Adjustable PWM Output Frequency
- I²C-Adjustable Output Current
  - 0 to 100mA Range
  - 97.7µA/LSB
  - 1 LSB DNL
  - ±7 LSB INL
  - ±2% FSR Gain Error
  - ±0.75% FSR Offset Error
- High Level of Integration for Performance
  - Slew-Rate Limiting and Spread-Spectrum Oscillator for Reduced EMI
  - I²C-Adjustable Output Transition Shaping for Mechanical Ringing Reduction
  - Open-/Short-Circuit Protection and Diagnostics
- Low Power Consumption
  - Low-Power Shutdown Mode 6µA (max)
- Minimize PCB Area
  - 2 x 3 Bump Package, 0.4mm Pitch 0.78mm x 1.35mm x 0.35mm

Typical Application Circuit



19-6041; Rev 0; 9/11

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND
V_{DD}.....-0.3V to +6.0V
ISOURCE, ISINK..... -0.6V to (V_{DD} + 0.6V)
SDA, SCL..... -0.3V to +6.0V
Continuous Current into V_{DD}, GND.....175mA
Continuous Current into ISOURCE, ISINK.....175mA

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 10.5mW/°C above +70°C).....570mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....95°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = +2.3V to +5.5V, R_{VCM} = 15Ω, L_{VCM} = 47µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.6V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Supply Voltage	V_{DD}		2.3		5.5	V
V_{DD} Shutdown Supply	I_{SH}	SCL = GND		3.1	6	µA
V_{DD} Standby Current	I_{STBY}	I_OUT[9:0] = 0		25	60	µA
V_{DD} Active Supply Current	I_{DD}	I_OUT[9:0] = 1		0.79		mA
Thermal Shutdown	T_{SHDN}			+150		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			+40		°C
UVLO Threshold	V_{UVLO}	Device in standby or active mode	2.0		2.3	V
Internal POR	V_{POR}		0.6		2.2	V
VOICE COIL OUTPUTS STATIC PERFORMANCE						
ISOURCE Output High On-Resistance	R_{HSH}	V_{DD} = 2.3V		0.72	1	Ω
		V_{DD} = 4.2V		0.48		
ISOURCE Output Low On-Resistance	R_{HSL}	V_{DD} = 2.3V		0.69	1.1	Ω
		V_{DD} = 4.2V		0.51		
ISINK Output Low On-Resistance	R_{LSL}	V_{DD} = 2.3V		1.2	1.85	Ω
		V_{DD} = 4.2V		1		
Resolution	N			10		Bits
LSB Size				97.7		µA
Integral Nonlinearity	INL	Linear mode; V_{DD} = 3.3V, I_OUT[9:0] = 0x028, 0x180, 0x300, 0x3FF (Notes 3, 4)	-7		+7	LSB

Electrical Characteristics (continued)

(V_{DD} = +2.3V to +5.5V, R_{VCM} = 15Ω, L_{VCM} = 47µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.6V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Nonlinearity	DNL	Linear mode (Note 3)	V_{DD} = 3.3V, T_A = +25°C	-1		+1	LSB
			V_{DD} = +2.3V to +5.5V, T_A = -40°C to +85°C	-1.5		+1.5	
Gain Error	G_{ERR}	I_OUT[9:0] = 0x333 (80mA); linear mode; V_{DD} = 3.3V (Notes 3, 4)	T_A = +25°C	-2		+2	%FSR
			T_A = -40°C to +85°C	-5		+5	
Offset Error	OFS	I_OUT[9:0] = 0x028 (3.91mA), linear mode, V_{DD} = 3.3V (Notes 3, 4)		-0.75		+0.75	%FSR
Short-Detection Threshold Current	I_{SHRT}	Source or sink current on ISOURCE and ISINK		200			mA
Diagnostic VCM Good Resistance Range	$R_{DIAGVCM}$	V_{DD} = 3.6V (Note 4)		5		50	Ω
VOICE COIL OUTPUTS DYNAMIC PERFORMANCE							
Output Switching Frequency	f_{OUT_0}	Spread-spectrum disabled; FREQ[2:0] = 000		1.205	1.35	1.536	MHz
	f_{OUT_1}	Spread-spectrum disabled; FREQ[2:0] = 001		1.818	2	2.222	
	f_{OUT_2}	Spread-spectrum disabled; FREQ[2:0] = 010		2.326	2.6	2.959	
	f_{OUT_3}	Spread-spectrum disabled; FREQ[2:0] = 011		3.300	3.79	4.464	
	f_{OUT_4}	Spread-spectrum disabled; FREQ[2:0] = 100		4.202	4.91	5.780	
Internal Clock Period	T_{CLK}	FREQ[2:0] = 001		1.350	1.5	1.650	µs
		FREQ[2:0] = 000 to 100		1.302	1.5	1.904	
Spread-Spectrum Bandwidth	Δf_{OUT}	FREQ[2:0] = 100			±20		%
PWM Output Rise Time	t_{PWMLH}	SRL = 0, I_{VCM} = 10mA			3.6		ns
	t_{PWMLH0}	SRL = 1, SR[2:0] = 000, I_{VCM} = 10mA			21		
	t_{PWMLH7}	SRL = 1, SR[2:0] = 111, I_{VCM} = 10mA			7.2		
PWM Output Fall Time	t_{PWMHL}	SRL = 0, I_{VCM} = 10mA			8.4		ns
	t_{PWMHL0}	SRL = 1, SR[2:0] = 000, I_{VCM} = 10mA			37		
	t_{PWMHL7}	SRL = 1, SR[2:0] = 111, I_{VCM} = 10mA			10.4		

Electrical Characteristics (continued)

(V_{DD} = +2.3V to +5.5V, R_{VCM} = 15Ω, L_{VCM} = 47µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.6V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Ripple	I_{RPL}	FREQ[2:0] = 001, measured peak to peak		16		%
Driver Efficiency	EFF	I_OUT[9:0] = 0x148 (~32mA)		64		%
Supply Voltage Feedthrough		I_OUT[9:0] = 0x148 (~32mA), measured with f_S = 217Hz, V_S = 200mV_{P-P}		3.5		LSB
Output Current Settling Time	t_{SV}	Any value to any other value transition, measured from I²C write complete to output settling within 10 LSB of final value, TSHP = 0 (Notes 4, 5)			250	µs
POWER STATE TIMING (Figure 1)						
Timeout to Detect SCL from Power-On	$t_{VBAT-GOOD}$	(Note 5)			150	µs
Time from Shutdown to Standby	t_{SH-ST}	(Note 5)			100	µs
Time from Standby to Active	t_{ST-A}	(Note 5)			250	µs
SCL Low Hold Time to Trigger Shutdown	t_{SCL-L}		740	769.5		µs
Time from Active to Standby	t_{A-ST}	(Note 5)			20	µs
Time from Standby to Shutdown	t_{ST-SH}	(Note 5)			20	µs
Time from Active to Shutdown	t_{A-SH}	(Note 5)			20	µs
CONTROL INPUTS (SDA, SCL)						
Input Logic-High Voltage	$V_{IH_}$		1.4			V
Input Logic-Low Voltage	$V_{IL_}$				0.4	V
Input Logic Hysteresis	V_{IHYS}			200		mV
Output Logic-Low Voltage	V_{OL}	I_{SINK} = 2mA			0.4	V
Input Low Leakage Current	$I_{IL_}$		-1		+1	µA
Input High Leakage Current	$I_{IH_}$		-1		+1	µA
Input Capacitance	C_{IN}			2		pF
I²C INTERFACE (Figure 6)						
Serial-Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between START and STOP Condition	t_{BUF}		0.5			µs

Electrical Characteristics (continued)

(V_{DD} = +2.3V to +5.5V, R_{VCM} = 15Ω, L_{VCM} = 47µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.6V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time for Repeated START Condition	$t_{HD:STA}$		0.26			µs
Low Period for SCL Clock	t_{LOW}		0.5			µs
High Period for SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated START Condition	$t_{SU:STA}$		0.26			µs
Data Hold Time	$t_{HD:DAT}$	(Note 5)	0			µs
Data Setup Time	$t_{SU:DAT}$	(Note 5)	50			ns
Rise Time of Both SDA and SCL Signals	t_r	(Note 5)			120	ns
Fall Time of Both SDA and SCL Signals	t_f	(Note 5)			120	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.26			µs
Capacitive Load for Each Bus Line	C_b	(Note 5)			400	pF
SCL/SDA Noise Suppression Time	t_I			50		ns
ESD PROTECTION						
All Pins		Human Body Model		±2		kV

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: Production tested in linear mode. Specification in PWM mode is guaranteed by design.
Note 4: Production tested at specified supply voltage. Specification over supply range is guaranteed by design.
Note 5: Not production tested; guaranteed by design.

Timing Diagram

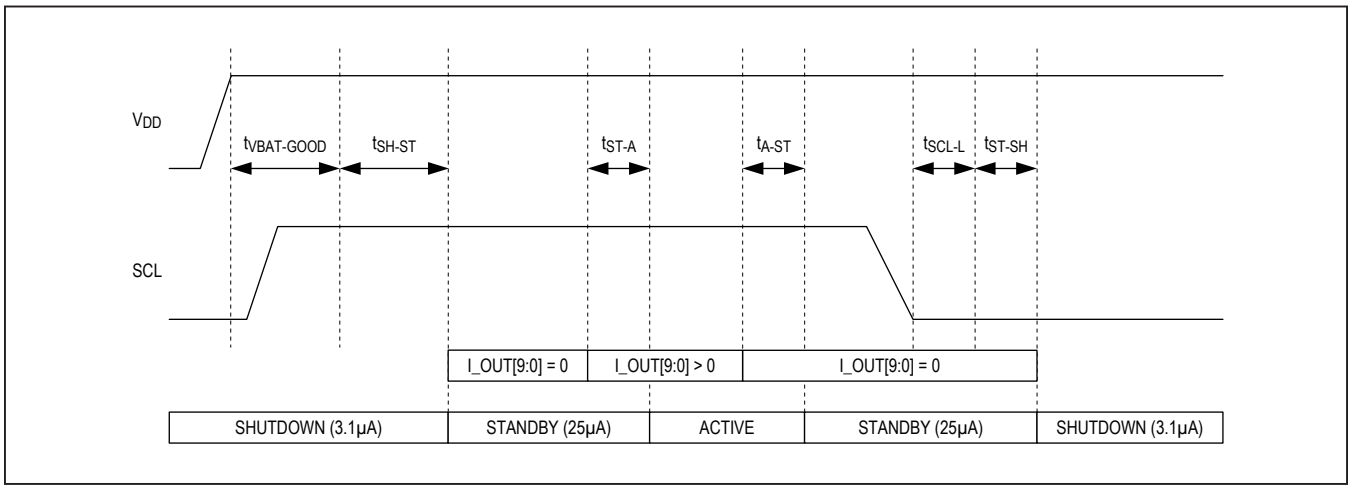
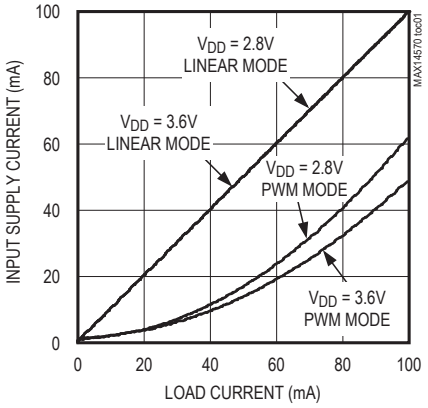


Figure 1. Power Mode Timing Details

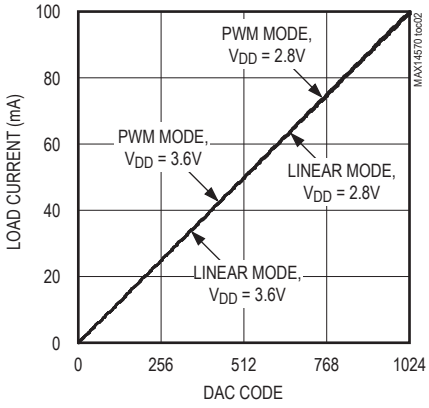
Typical Operating Characteristics

(V_{DD} = +3.6V, T_A = +25°C, load resistor = 15Ω, inductor = 47µH, frequency = 2MHz, PWM mode unless otherwise noted.)

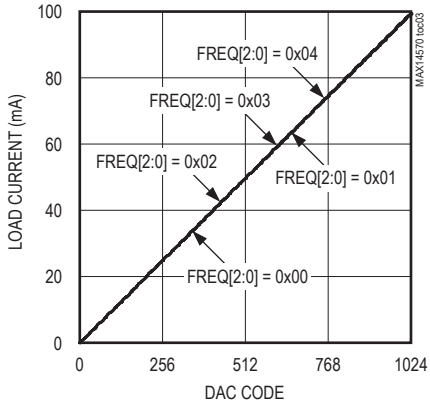
INPUT SUPPLY CURRENT vs. LOAD CURRENT



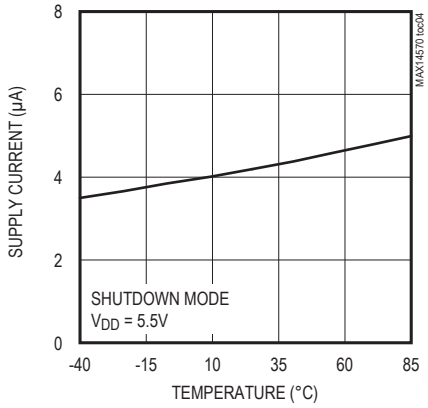
LOAD CURRENT vs. DAC CODE



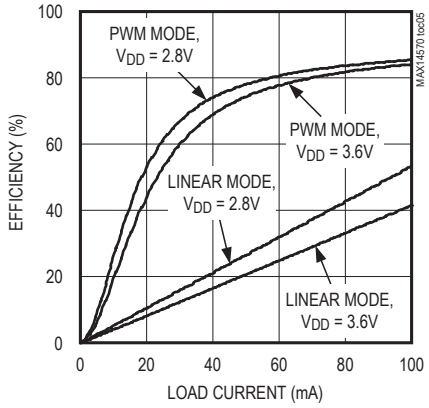
LOAD CURRENT vs. DAC CODE



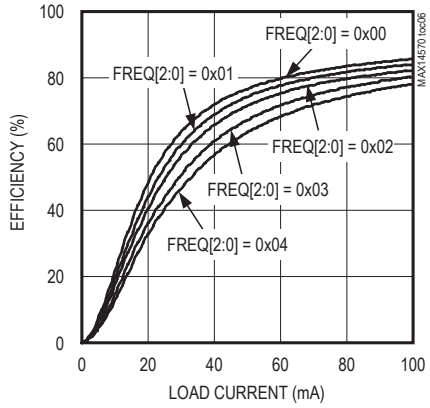
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



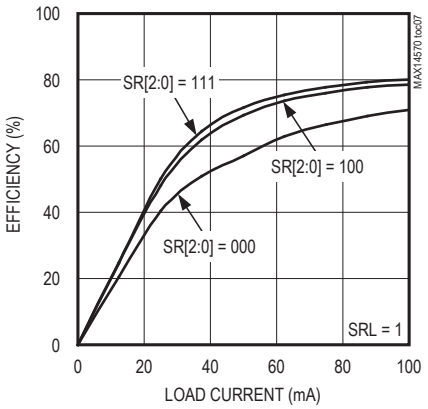
EFFICIENCY vs. LOAD CURRENT



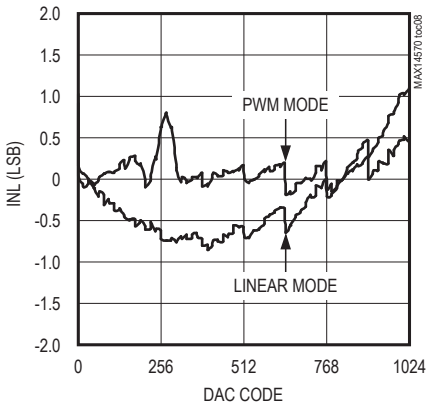
EFFICIENCY vs. LOAD CURRENT



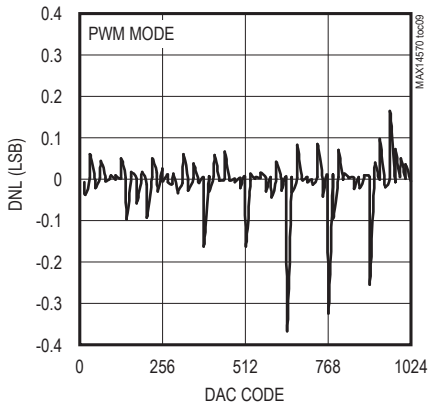
EFFICIENCY vs. LOAD CURRENT



INL vs. CODE



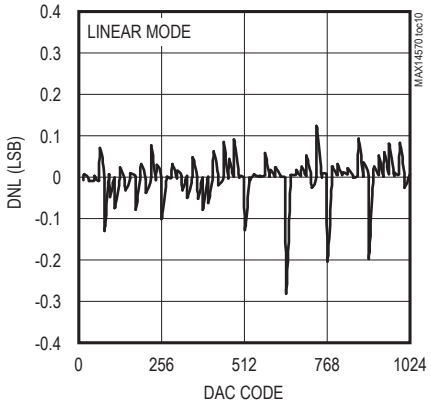
DNL vs. CODE



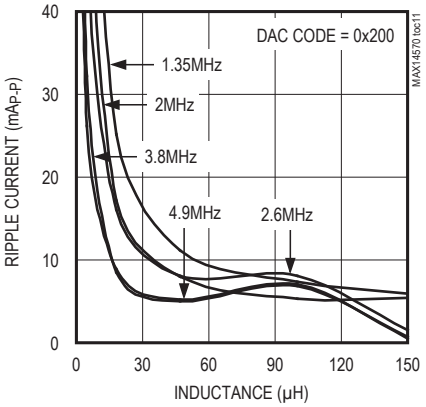
Typical Operating Characteristics (continued)

(V_{DD} = +3.6V, T_A = +25°C, load resistor = 15Ω, inductor = 47µH, frequency = 2MHz, PWM mode unless otherwise noted.)

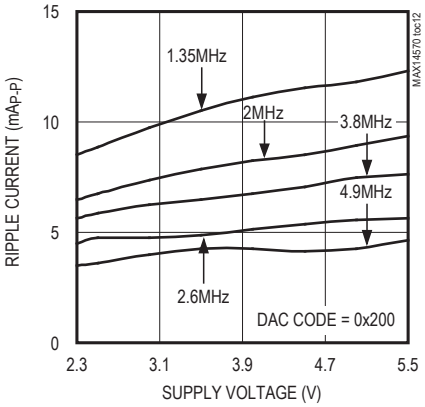
DNL vs. CODE



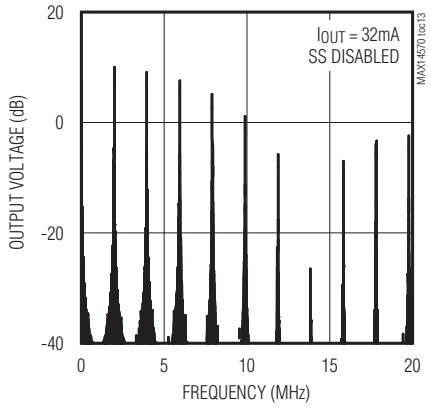
RIPPLE CURRENT vs. INDUCTANCE



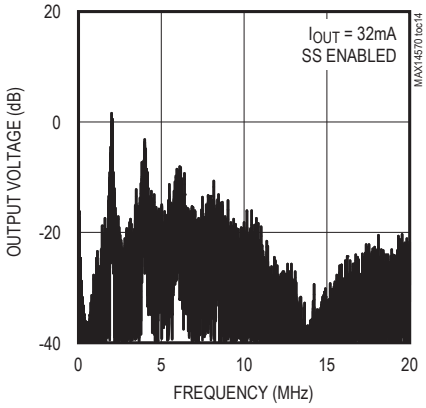
RIPPLE CURRENT vs. SUPPLY VOLTAGE



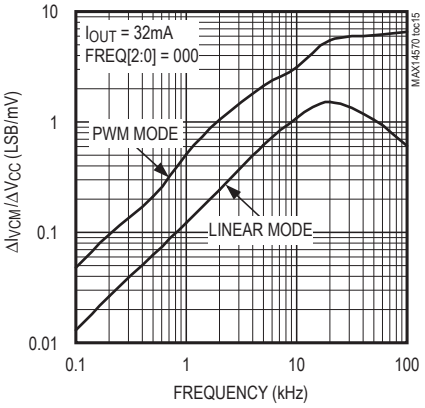
OUTPUT FFT



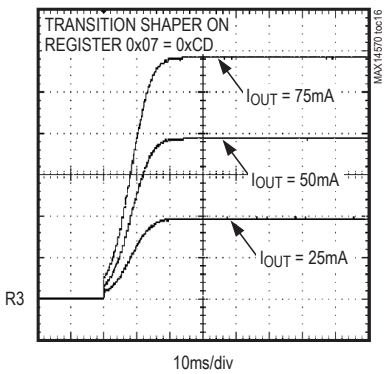
OUTPUT FFT



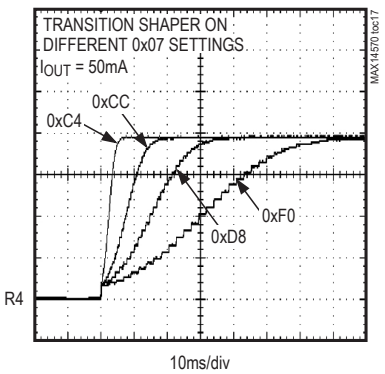
POWER-SUPPLY FEEDTHROUGH vs. FREQUENCY



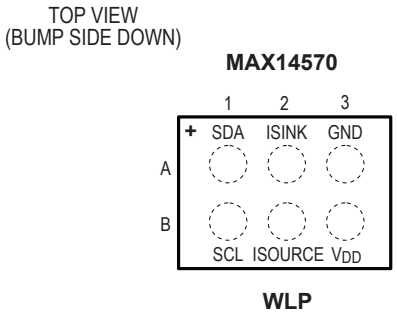
OUTPUT TRANSITION



OUTPUT TRANSITION



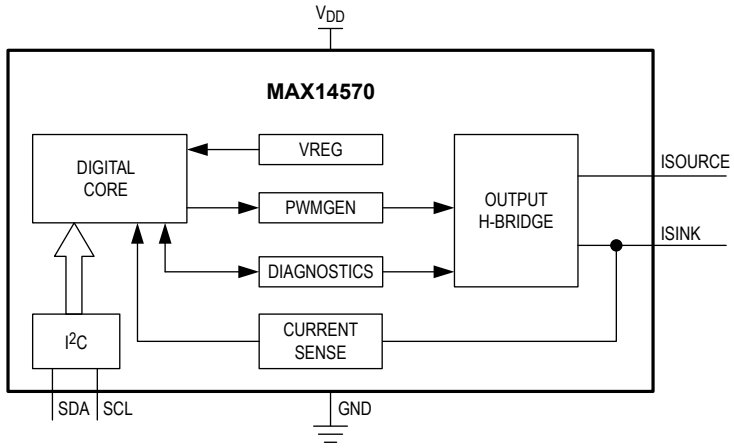
Bump Configuration



Bump Description

BUMP	NAME	FUNCTION
A1	SDA	I²C Open-Drain Serial Data Input/Output
A2	ISINK	Voice Coil Current Sink. Connect ISINK to low side of voice coil.
A3	GND	Ground
B1	SCL	I²C Open-Drain Serial Clock Input
B2	ISOURCE	Voice Coil Current Source. Connect ISOURCE to high side of voice coil.
B3	V_{DD}	Input Supply Voltage from 2.3V to 5.5V. Bypass V_{DD} to GND with a 0.1µF capacitor.

Functional Diagram



Detailed Description

The MAX14570 voice coil motor (VCM) driver utilizes an integrated H-bridge to provide a high-efficiency VCM driver solution. This device features a 10-bit DAC controlled by a simple 2-wire I²C interface to set the DC current through the voice coil outputs.

Power-On Reset

When the MAX14570 initially powers up, all the registers are cleared and the device is in shutdown mode.

Coil Outputs (ISOURCE, ISINK)

The MAX14570 regulates current through a VCM load connected between ISOURCE and ISINK using a switching regulator or a linear regulator (see register 0x06). Either a pulse-width modulated (PWM) signal or a constant current source drives the ISOURCE output. The ISINK input senses flowing current.

PWM Output Mode

When PWM output mode is enabled, the ISOURCE pin switches at high frequency between V_{DD} and GND. The Mode register (0x06) sets the frequency of the PWM signal. The duty cycle automatically adjusts to regulate the average output current to the programmed value in I_OUT[9:0].

EMI Reduction in PWM Mode

In PWM mode, the sharp transitions can cause electromagnetic interference (EMI) that is harmful to other circuitry. The MAX14570 includes two features designed to reduce this effect.

An adjustable slew-rate limiting feature can be enabled in the Switching Output Slew Rate register (0x08) to reduce EMI and conducted emissions output. The slew-rate limiting feature lowers the efficiency of the PWM driver when it is enabled (see the *Typical Operating Characteristics*).

Spread-spectrum output clocking, enabled in the Mode register (0x06), further reduces EMI. In spread-spectrum mode, the output frequency randomly varies within ±20% of the center frequency to reduce peak EMI spectral energy.

Power-Mode Control (Figure 1)

The MAX14570 uses three types of working modes: shutdown, standby, and active.

The device is in shutdown mode after power-on reset (POR), reducing supply current to the lowest possible amount. The device exits shutdown mode and enters standby mode after the $t_{VBAT-GOOD}$ timeout period, and the SCL line is pulled high. When a non-zero code is programmed into I_OUT[9:0], the device enters active mode and begins powering the VCM.

The device enters shutdown mode when the SCL line is held low for longer than the specified hold time (t_{SCL-L}), regardless of the value in I_OUT[9:0]. The device can enter shutdown from standby or active mode. Upon entering shutdown, all I²C registers are reset to their default power-up value.

Shutdown Mode

The MAX14570 enters shutdown mode when the SCL line is held low for longer than the specified hold time (t_{SCL-L}). ISOURCE, ISINK, and SDA are high impedance in shutdown mode, and all I²C registers are reset to default values. After a valid I²C START, entering shutdown is disabled until a valid I²C STOP is received. The lowest possible amount of power is consumed while in shutdown mode.

Standby Mode

When the device is not in shutdown mode and 0x000 is programmed into I_OUT[9:0], the device enters standby mode. During standby mode, all circuitry is disabled except for the UVLO and I²C interface.

ISOURCE and ISINK are high impedance in standby mode, and power consumption is reduced.

Standby mode is the preferred mode to change the PWM frequency or to change between PWM output and linear output.

Active Mode

Active mode is entered whenever the VCM is being driven. ISINK is driven low and ISOURCE is driven either with a PWM signal or with a continuous current according to the PWM_LIN bit in the Mode register.

Undervoltage Lockout

Internal UVLO circuitry monitors the V_{DD} power supply. Any time V_{DD} drops below the UVLO threshold, the I²C registers reset to their default state and I²C communications are ignored. I²C communications can resume when V_{DD} rises above the UVLO threshold.

Ringing Compensation

When the MAX14570 is used to drive a VCM motor, an internal digital shaper can be enabled to shape the output current step to reduce mechanical ringing and speed up actuator settling time (see Figure 2 and Figure 3).

The digital shaper reconstructs the step response of a lowpass filter. The equivalent cutoff frequency, f_0, is dependent on the internal clock period and can be selected by the Transition Shaper Cutoff Frequency register. The cutoff frequency can be expressed by the following equation:

$$f_0 \approx \frac{0.01683}{4 \times 2^{FSHPD} \times FSHP \times T_{CLK}}$$

where T_{CLK} = 1.5µs (typ), and FSHPD and FSHP are decimal converted values from the Transition Shaper Cutoff Frequency register.

The following formula can be used to approximate the optimal cutoff frequency for a specific VCM:

$$f_0 < \frac{f_{VCM}}{4}$$

Note that the relationship between cutoff frequency and VCM resonance frequency varies with VCM actuator parameters such as the damping factor. Some margin should be provided for lowpass filter variation and VCM resonant frequency variation to guarantee stable performance. Use a cutoff frequency slightly **lower** than the optimal to ensure that there is no actuator ringing at the resonant frequency of the VCM, and the settling time is not too slow.

A more detailed optimization is suggested for optimal performance that requires two values:

T_O = oscillation frequency of the VCM. The resonance frequency (T_{RES}) and oscillation frequency are not exactly the same for a damped oscillator; however, they are approximately equal for small damping factors.

D_{VCM} = damping factor of the VCM.

Use the following procedure to extract these values from a plot of the VCM step response and set f_0;

1) Apply a step input to the VCM and capture the response. Ensure that the step response overshoot and ringing remains in the linear region of VCM operation.
2) Measure the period of the oscillation directly based on 3–4 periods.
3) Measure the peak-to-peak free-oscillation amplitude on two different points of the waveform. Skip the first period to ensure that any distortion does not affect the measurement. Take the two points 3–4 periods apart.

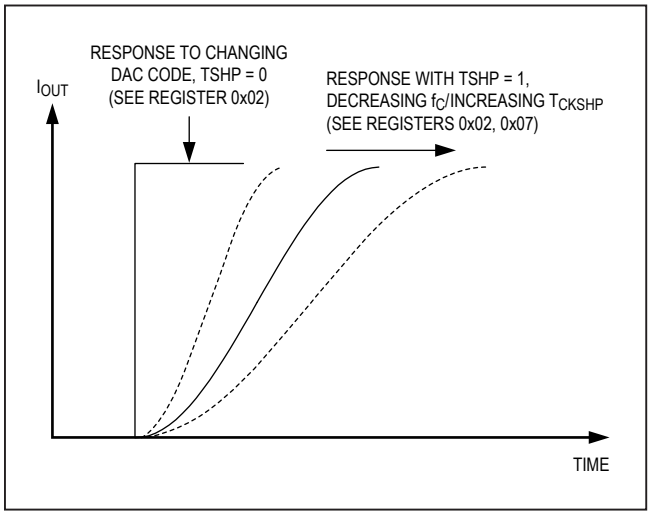


Figure 2. Output Response to Changing DAC Code for Different TSHP Settings

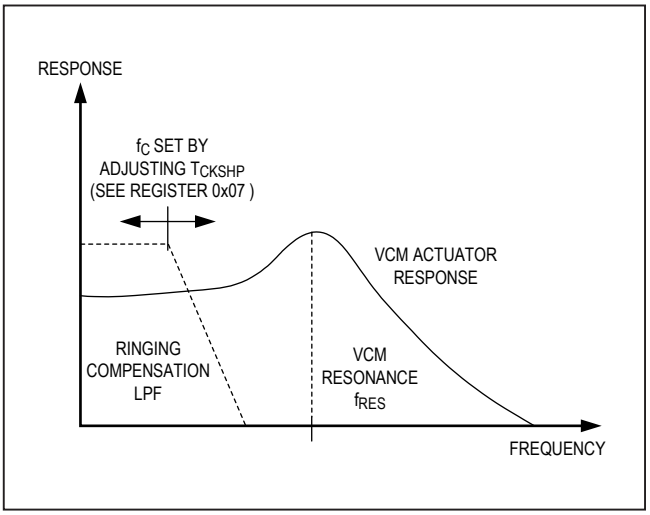


Figure 3. Frequency Domain Adjustment of Lowpass Filter Using FSHP and FSHPD Bits

4) D_{VCM} can be approximated from this information only for small values of D_{VCM}. The step response oscillates heavily in this case. Use the following equations to approximate D_{VCM} and T_O:

$$D_{VCM} \approx \frac{\ln\left(\frac{V_{PP1}}{V_{PP2}}\right)}{2\pi \times N_C}$$

$$T_O \approx T_{RES}$$

where N_C is the number of periods between the measured peak-to-peak values.

5) Use the chart in Figure 4 to extrapolate the suggested $f_0 \times T_O$ product.

6) Divide this product by T_O to determine the maximum limit for f_0.

7) Apply 10% margin.

A slightly higher f_0 can be used for applications with step sizes that are always larger than 2mA. This is due to the limitation of digital shaper resolution for very small step sizes.

Below is an example calculation for setting f_0 based on the step response of a VCM shown in Figure 5.

1) VCM step response shown in Figure 5.
2) Δt = 52.4ms
3) V_{PP1} = 2.3 divisions, V_{PP2} = 1.8 divisions.
4) $D_{VCM} \approx 0.00975$, $T_O \approx 13.1$ms.
5) $D_{VCM} \approx 0.01$ corresponds to $f_0 \times T_O = 0.37$
6) f_0 (optimal) = 0.37/13.1ms = 28.2Hz
7) f_0 (safe) = 28.2Hz x 90% = 25.4Hz

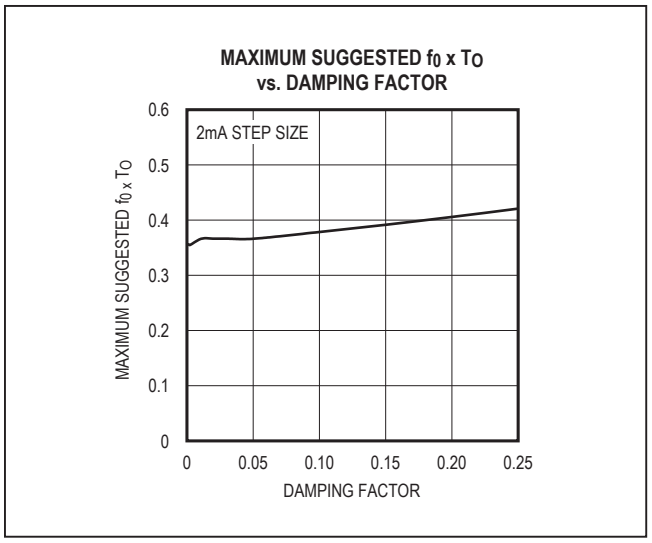


Figure 4. Maximum $f_0 \times T_O$ Product vs. D_{VCM}

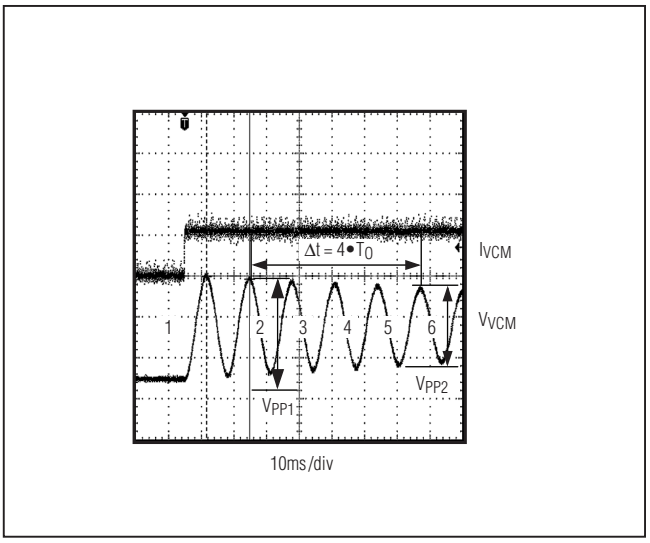


Figure 5. Step Response of Sample VCM

Voice Coil Diagnostics

The MAX14570 ISOURCE and ISINK outputs are internally protected against overcurrent, short circuit to V_{DD} or GND, and open-load conditions. Diagnostics mode can be entered to check for any of these conditions and report back to the host controller. Diagnostics are enabled by setting the DIAG bit to 1 in the Status (0x05) register. The SHORT bit is asserted when ISOURCE is shorted to ISINK, or if either output is shorted to GND or V_{DD}. The OPEN bit is asserted when there is no current path between ISOURCE and ISINK. The PROT bit is asserted when there is an overcurrent into ISOURCE or ISINK pins. See the *Register Definitions* section for more information.

While in diagnostics mode, the VCM is not being driven by the value programmed into I_OUT[9:0]; it is instead driven by a 6mA diagnostic current.

Loop Compensation

The stability of the current loop in switching mode is related to the load used. The error amplifier inserts a programmable zero in the loop gain to compensate the first electrical pole of the load. Set the time constant of this zero based on the time constant of the load (see Table 1).

Table 1. Compensation Bits Setting

LOAD ELECTRICAL TIME CONSTANT (L/R)	SUGGESTED COMP[1:0] SETTING
2.5µs to 5.7µs	00
5.7µs to 13µs	01
13µs to 29µs	10
29µs to 200µs	11

Register Map

(All default reset values are 0x00 unless otherwise noted.)

REGISTER	ADDR	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Manufacturer and Chip ID	0x00	R	MID3	MID2	MID1	MID0	CID3	CID2	CID1	CID0
Version ID	0x01	R	RES*	RES*	RES*	RES*	VERID3	VERID2	VERID1	VERID0
System Control	0x02	R/W	X	X	X	X	X	X	TSHP	SW_RES
Output Current MSB	0x03	R/W	X	X	X	X	X	X	I_OUT9	I_OUT8
Output Current LSB	0x04	R/W	I_OUT7	I_OUT6	I_OUT5	I_OUT4	I_OUT3	I_OUT2	I_OUT1	I_OUT0
Status	0x05	R/W	X	X	DIAG	THRM (read only)	SHORT (read only)	OPEN (read only)	X	PROT
Mode	0x06	R/W	RETRY	SS	X	FREQ2	FREQ1	FREQ0	PWM_LIN	X
Transition Shaper Cutoff Frequency	0x07	R/W	FSHPD1	FSHPD0	FSHP5	FSHP4	FSHP3	FSHP2	FSHP1	FSHP0
Switching Output Slew Rate	0x08	R/W	RES*	RES*	COMP1	COMP0	SRL	SR2	SR1	SR0

RES = Reserved Bits. Must be set to 0.*

X = Don't Care.

Register Definitions

FIELD NAME	READ/WRITE	BITS	POWER-ON RESET	DESCRIPTION
Manufacturer and Chip ID (I^2C Address = 0x00)				
MID[3:0]	Read	[7:4]	0110	Manufacturer Identification
CID[3:0]	Read	[3:0]	0001	Chip Identification
Version ID (I^2C Address = 0x01)				
VERID[3:0]	Read	[3:0]	0001	Version Identification
System Control (I^2C Address = 0x02)				
TSHP	Read/ Write	1	0	Set TSHP = 1 to enable the ringing compensation transition shaper. Set TSHP = 0 to disable the ringing compensation transition shaper.
SW_RES	Read/Write	0	0	Set SW_RES = 1 to reset all registers to power-up values and place the device into standby mode. The device forces all I^2C registers (except the SW_RES bit) to the POR value
Output Current MSB (I^2C Address = 0x03)				
I_OUT[9:8]	Read/Write	[1:0]	00	These are the two most significant bits of the 10-bit I_OUT[9:0] linearly scaled average current in the voice coil actuator. I_OUT[9:0] = 0x000 = switching output disabled (standby mode) I_OUT[9:0] = 0x3FF = 100mA I_OUT[9:0] has a linear scale with LSB size of 97.7µA/LSB. The DAC output updates only after a complete multibyte write to 0x03 and 0x04. I.e., if only register 0x03 is written, the DAC output does not update with the new data.
Output Current LSB (I^2C Address = 0x04)				
I_OUT[7:0]	Read/Write	[7:0]	00000000	These are the eight least significant bits of the 10-bit I_OUT[9:0] linearly scaled average current in the voice coil actuator. I_OUT[9:0] = 0x000 = switching output disabled (standby mode) I_OUT[9:0] = 0x3FF = 100mA I_OUT[9:0] has a linear scale with LSB size of 97.7µA/LSB. The DAC output updates only after a complete multibyte write to 0x03 and 0x04. I.e., if only register 0x03 is written, the DAC output does not update with the new data.
Status (I^2C Address = 0x05)				
DIAG	Read/Write	5	0	Set DIAG = 1 to check for open-/short-circuit conditions on the VCM driver outputs. The result of the diagnostic appears in the SHORT and OPEN bits 1ms after DIAG is set to 1.
THRM	Read	4	0	THRM is set to 1 and the device enters a nonoperative mode if the die temperature exceeds +150°C (typ). The THRM bit is cleared and the device resumes normal operation when the die temperature decreases to less than +110°C (typ).
SHORT	Read	3	0	SHORT is set to 1 if there is a short between ISOURCE and ISINK or from either output to V_{DD} or GND. SHORT is only functional when DIAG = 1. When DIAG = 0, SHORT = 0.
OPEN	Read	2	0	OPEN is set to 1 if there is no current path between ISOURCE and ISINK. OPEN is only functional when DIAG = 1. When DIAG = 0, OPEN = 0.

Register Definitions (continued)

FIELD NAME	READ/WRITE	BITS	POWER-ON RESET	DESCRIPTION
PROT	Read	0	0	PROT is set to 1 and the device enters a nonoperative mode if an overcurrent condition is detected. In this mode, the outputs are high impedance. If RETRY = 1, then every 100ms the device automatically tries to return to an operative mode. Once the overcurrent is no longer detected, the PROT bit is reset to 0. If RETRY = 0, the device remains in a nonoperative mode until standby mode is entered (I_OUT[9:0] = 0x000 or SW_RESET = 1).
Mode (I^2C Address = 0x06)				
RETRY	Read/Write	7	0	Autoretry Control for Overcurrent Protection. See the PROT bit description.
SS	Read/Write	6	0	Set SS = 1 to enable the spread-spectrum switching output oscillator. Set SS = 0 to disable the spread-spectrum output oscillator and use fixed-frequency mode.
FREQ[2:0]	Read/Write	[4:2]	000	FREQ[2:0] sets the output switching frequency of the PWM driver. The internal clock frequency for the ringing compensation transition shaper is derived from this frequency. 000 = 1.4MHz $T_{CLK} = 2/f_{PWM}$ 001 = 2.0MHz $T_{CLK} = 3/f_{PWM}$ 010 = 2.6MHz $T_{CLK} = 4/f_{PWM}$ 011 = 3.8MHz $T_{CLK} = 6/f_{PWM}$ 100 = 4.9MHz $T_{CLK} = 8/f_{PWM}$
PWM_LIN	Read/Write	1	0	Set PWM_LIN = 0 to enable PWM output mode. Set PWM_LIN = 1 to enable linear output mode.
Transition Shaper Cutoff Frequency (I^2C Address = 0x07)				
FSHPD[1:0]	Read/Write	[7:6]	00	Ringing Compensation Transition Shaper Clock Prescaler. These bits set the course divider value of the digital shaper clock. See the *Detailed Description* for more information.
FSHP[5:0]	Read/Write	[5:0]	000000	Ringing Compensation Transition Shaper Clock Divider. See the *Detailed Description* for more information.
Switching Output Slew Rate (I^2C Address = 0x08)				
COMP[1:0]	Read/Write	[5:4]	00	These bits are used to tune the control loop filter in PWM mode (PWM_LIN = 0) for particular VCM inductance/resistance values to ensure stability of the loop filter. 00: τ_Z = 2.5µs 01: τ_Z = 5.7µs 10: τ_Z = 13µs 11: τ_Z = 29µs
SRL	Read/Write	3	0	Set SRL = 1 to enable slew-rate limiting of the switching output waveform. Set SRL = 0 to disable slew-rate limiting of the switching output waveform.
SR[2:0]	Read/Write	[2:0]	000	SR[2:0] = 0x00 = Minimum output slew rate SR[2:0] = 0x07 = Maximum output slew rate See the *Electrical Characteristics* section for detailed slew-rate values.

Serial Addressing

The MAX14570 operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX14570 and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX14570 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 6).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 7). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 8). The data on SDA must remain stable while SCL is high.

I²C Serial Interface

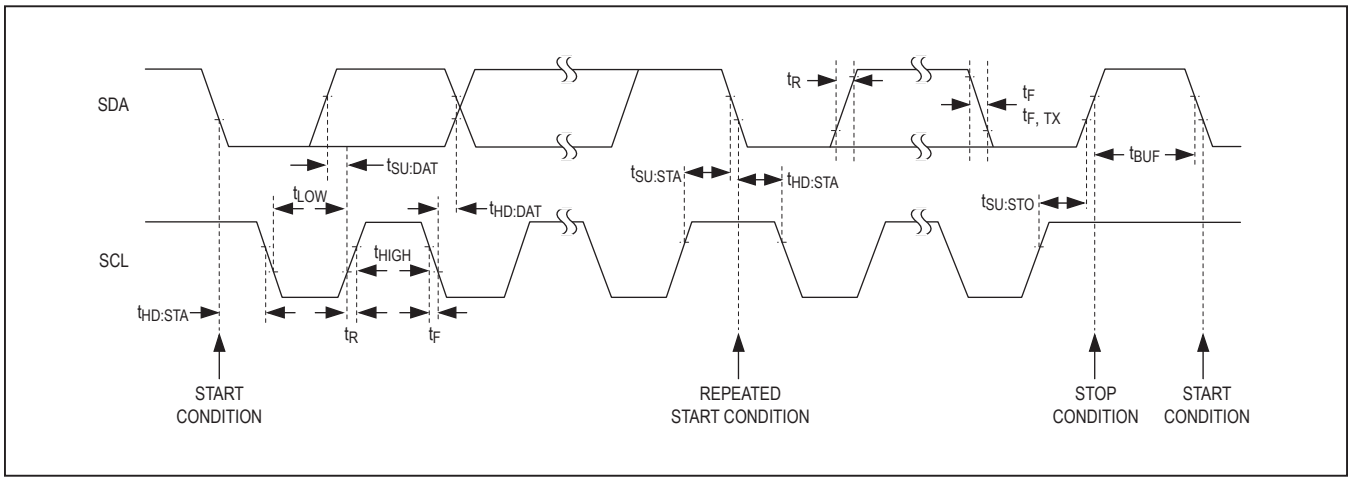


Figure 6. I²C Interface Timing Details

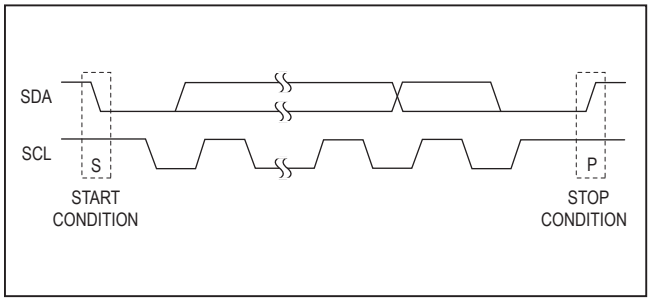


Figure 7. START and STOP Conditions

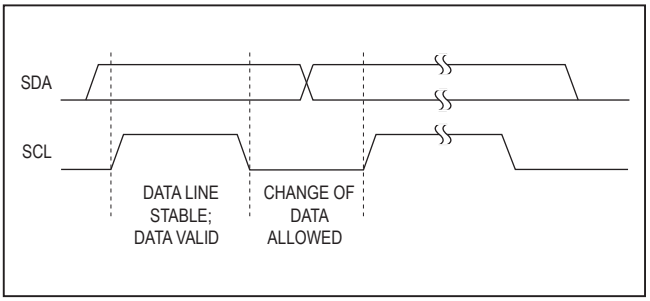


Figure 8. Bit Transfer

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit (Figure 9), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14570, it generates the acknowledge bit because the MAX14570 is the recipient. When the MAX14570 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. Note that when reading data from the MAX14570, always send a not-acknowledge (NACK) from the master on the last read data byte or the MAX14570 will not relinquish the bus.

Slave Address

The MAX14570 has a 7-bit long slave address. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address is 0x1C for write commands and 0x1D for read commands (Figure 10).

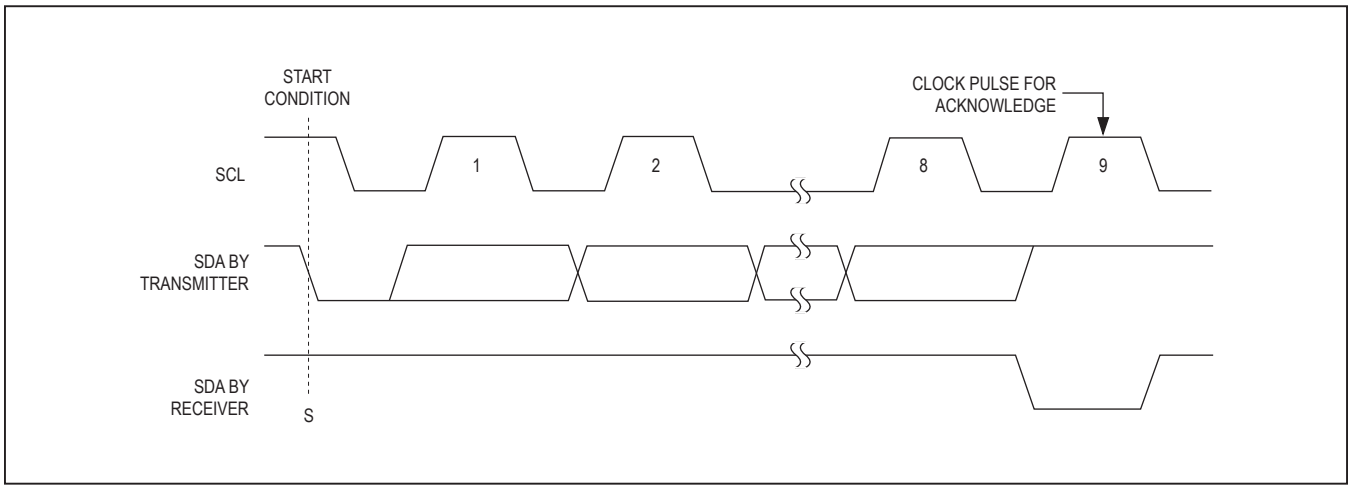


Figure 9. Acknowledge

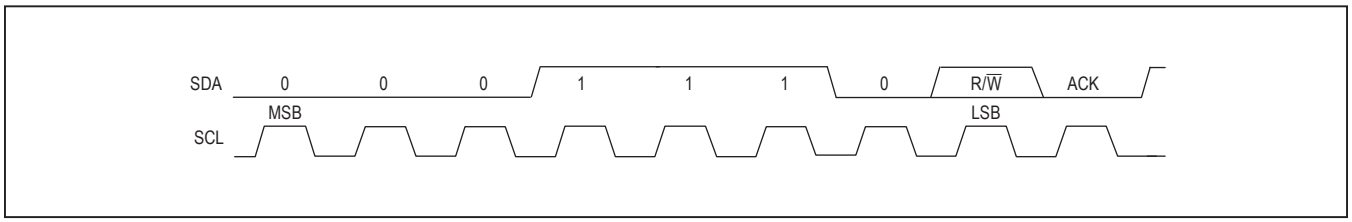


Figure 10. Slave Address

Format for Writing

To write to the MAX14570, the master generates a START condition and then transmits the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 data byte. The first data byte is the register address; this determines which register is to be written. The MAX14570 asserts an ACK on SDA if a valid register address is detected.

A data byte received after the register address goes into the selected register. For each additional byte received from the master, the MAX14570 autoincrements the register address. After all bytes are written, the master generates a STOP condition. Figure 11 shows a single register I2C write, and Figure 12 shows a multiple register I2C write.

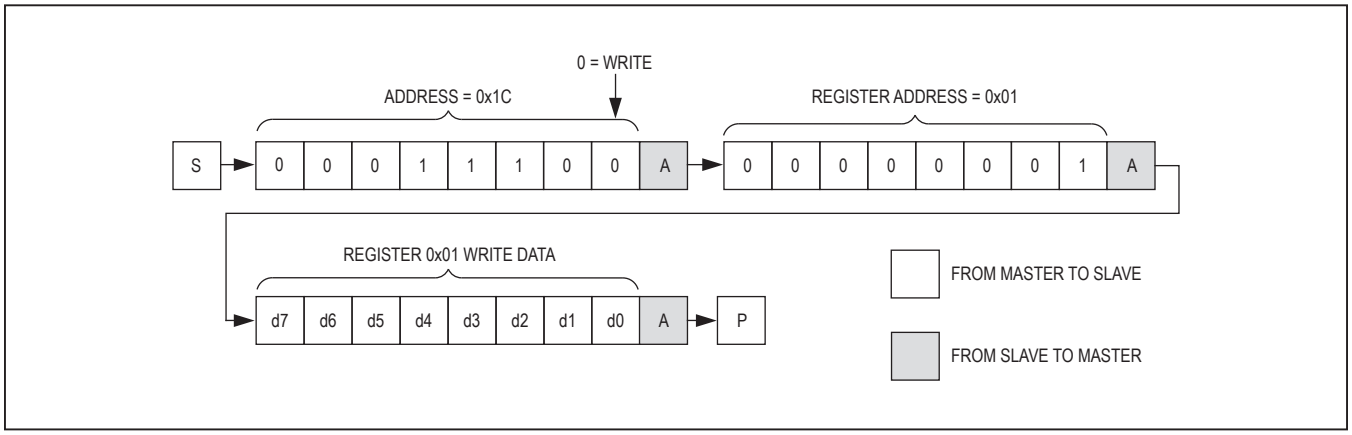


Figure 11. Format for I2C Write

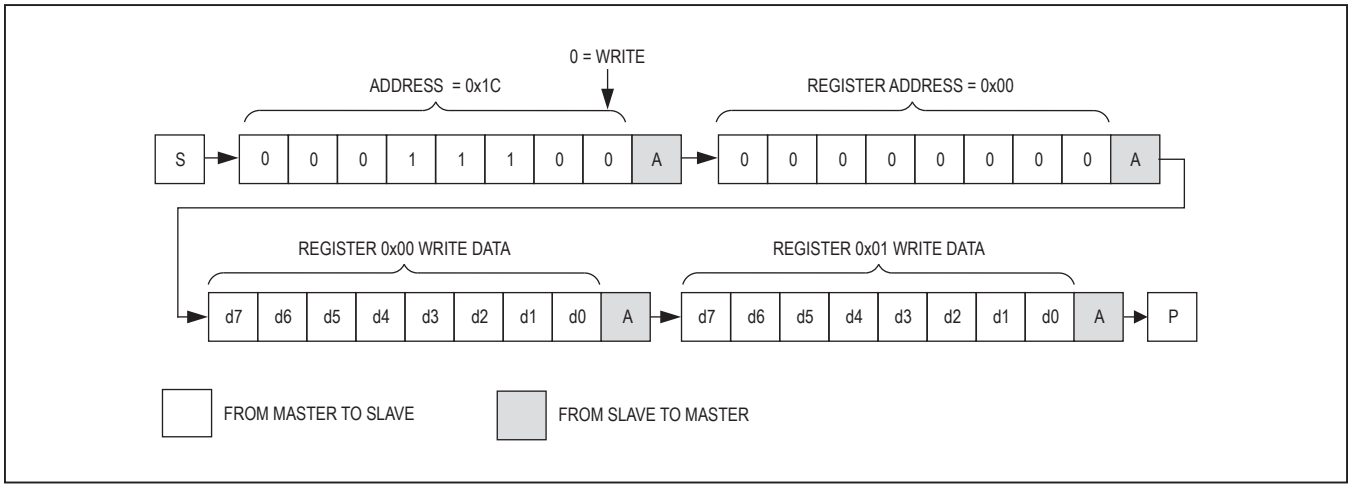


Figure 12. Format for Writing to Multiple Registers

Format for Reading

To read from the MAX14570, the master generates a START condition and then transmits the slave address with the R/$\overline{W}$ bit set to zero. The master then sends the register address to be read. After the MAX14570 asserts an ACK on SDA, the master sends a repeated START condition followed by the slave address with the R/W bit set to one. The MAX14570 then sends an ACK followed by the byte contained in the register. The device autoincrements the register address, and if the master asserts an ACK, the MAX14570 sends the next byte. To end the read transaction, the master must generate a NACK followed by a STOP condition. Figure 13 shows a single register read operation.

Applications Information

PCB Layout

Ensure that the GND and ISOURCE/ISINK connections are routed with thick traces to minimize parasitic resistance. High parasitic resistance can limit the maximum current delivered to the VCM.

When the device is operating in PWM output mode, the ISOURCE and ISINK lines switch at high frequencies. The ISOURCE voltage switches between the full amplitude of V_{DD} to GND, and the ISINK voltage is a filtered and out-of-phase version of this waveform due to the VCM coil properties. Therefore, route the ISOURCE and ISINK traces away from sensitive analog and digital supply lines.

Power-Supply Decoupling

In most applications, a 0.1µF bypass capacitor placed close to the V_{DD} pin provides adequate bypassing. However, larger capacitors can be used to minimize ripple on the V_{DD} line if necessary. Additionally, utilizing the slew-rate limiting feature can help to provide additional reduction of supply ripple.

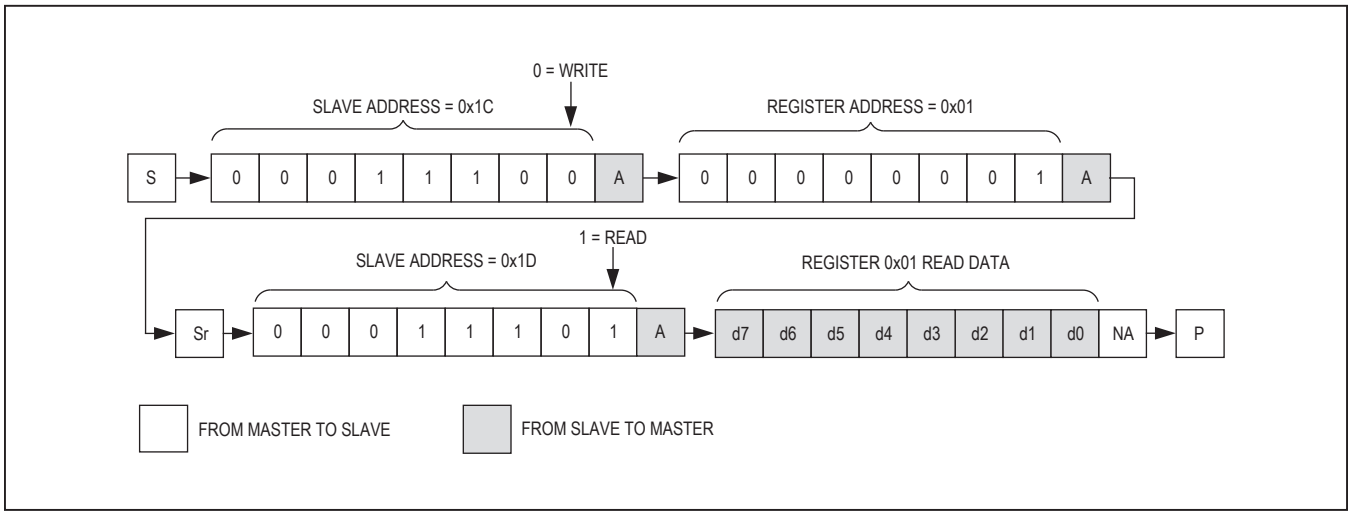


Figure 13. Format for Reading

Ordering Information

PART	TOP MARK	TEMP RANGE	PIN-PACKAGE
MAX14570EZT+T	AA	-40°C to +85°C	6 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 WLP	Z60A1+1	**21-0549**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/11	Initial release	—

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